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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,130	01/29/2004	Gurupada Mandal	SUN030155	7184

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Philip J. McKay
Gunnison, McKay & Hodgson, L.L.P.
Suite 220
1900 Garden Road
Monterey, CA 93940

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/769,130	MANDAL, GURUPADA
	Examiner	Art Unit
	Michael t. Tran	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *January 29, 2004 through November 15, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-9,12-14 and 18-20* is/are rejected.

7)☒ Claim(s) *4-6,10,11,15-17,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

MICHAEL TRAN
PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communications dated January 29, 2004 through November 15, 2004, claims 1-22 are active in this application.

Claim Objections

2. Claims 4-6, 10, 11, 15-17, 21 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1-3 are rejected under 35 U.S.C 102(b) as being anticipated by Miyatake

[U.S. Patent #5,255,235].

With respect to claim 1, Miyatake discloses, in figure 6, a boosted memory array comprising: at least one bitline [/BL]; at least one memory cell coupled to said bitline [6]; a bitline booster circuit [SA] coupled to said bitline; a bitline booster circuit bitline boost enable signal input terminal [terminal where signal S is coupled to] coupled to said bitline booster circuit; a bitline boost enable signal [S] coupled to said bitline booster circuit bitline boost enable signal input terminal, wherein, when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline [see col. 2, lines 30-45].

With respect to claim 2, Miyatake discloses, in figure 6, that the boosted memory array includes at least two bitlines, a first bitline [BL] and a second bitline [/BL].

With respect to claim 3, Miyatake discloses, in figure 7, that signal S is high when the wordline and bitline are high; hence, it is reasonable to interpret that the bitline boost enable signal [S] is active only during write operation.

5. Claims 7-9 is rejected under 35 U.S.C 102(b) as being anticipated by Miyatake [U.S. Patent #5,255,235].

With respect to claim 7, Miyatake discloses, in figure 6, a microprocessor chip [Miyatake inidicated that the device is applicable to a DRAM], said microprocessor chip comprising: one or more functional blocks [precharge/equalizer, decoders, buffers – see figure 1]; and a boosted memory array, said boosted memory array comprising: at least one bitline [/BL]; at least one memory cell coupled to said bitline [6]; a bitline booster

circuit [SA] coupled to said bitline; a bitline booster circuit bitline boost enable signal input terminal [terminal where signal S is coupled to] coupled to said bitline booster circuit; a bitline boost enable signal [S] coupled to said bitline booster circuit bitline boost enable signal input terminal, wherein, when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline [see col. 2, lines 30-45].

With respect to claim 8, Miyatake discloses, in figure 6, that the boosted memory array includes at least two bitlines, a first bitline [BL] and a second bitline [/BL].

With respect to claim 9, Miyatake discloses, in figure 7, that signal S is high when the wordline and bitline are high; hence, it is reasonable to interpret that the bitline boost enable signal [S] is active only during write operation.

6. Claims 12-14 are rejected under 35 U.S.C 102(b) as being anticipated by Miyatake [U.S. Patent #5,255,235].

With respect to claim 12, Miyatake discloses, in figure 6 and column 2, lines 30-45, a method for boosting the performance of a memory array comprising: providing at least one bitline [/BL]; coupling at least one memory cell [6] to said at least one bitline; coupling a bitline booster circuit [SA] to said at least one bitline; coupling a bitline booster circuit bitline boost enable signal input terminal [terminal where signal S is coupled to] to said bitline booster circuit; couping a bitline boost enable signal [S] to said bitline booster circuit bitline boost enable signal input terminal, such that; when said bitline boost enable signal is active and a signal on said at least one bitline starts going

low, said bitline booster circuit discharges said at least one bitline [see col. 2, lines 30-45].

With respect to claim 13, Miyatake discloses, in figure 6, that the boosted memory array includes at least two bitlines, a first bitline [BL] and a second bitline [/BL].

With respect to claim 14, Miyatake discloses, in figure 7, that signal S is high when the wordline and bitline are high; hence, it is reasonable to interpret that the bitline boost enable signal [S] is active only during write operation.

7. Claims 18-20 are rejected under 35 U.S.C 102(b) as being anticipated by Miyatake [U.S. Patent #5,255,235].

With respect to claim 18, Miyatake discloses, in figure 6, a method for improving the performance of a microprocessor chip [Miyatake inidicated that the device is applicable to a DRAM], said method comprising: providing one or more functional blocks [precharge/equalizer, decoders, buffers – see figure 1] on said microprocessor chip; providing a boosted memory array, said boosted memory array comprising: at least one bitline [/BL]; at least one memory cell coupled to said bitline [6]; a bitline booster circuit [SA] coupled to said bitline; a bitline booster circuit bitline boost enable signal input terminal [terminal where signal S is coupled to] coupled to said bitline booster circuit; a bitline boost enable signal [S] coupled to said bitline booster circuit bitline boost enable signal input terminal, wherein, when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline [see col. 2, lines 30-45].

With respect to claim 19, Miyatake discloses, in figure 6, that the boosted memory array includes at least two bitlines, a first bitline [BL] and a second bitline [/BL].

With respect to claim 20, Miyatake discloses, in figure 7, that signal S is high when the wordline and bitline are high; hence, it is reasonable to interpret that the bitline boost enable signal [S] is active only during write operation.

Allowable Subject Matter

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- A second transistor, an output of said second NOR gate being coupled to a control electrode of said second transistor, a first flow electrode of said second transistor being coupled said second bitline, a second flow electrode of said second transistor being coupled to said supply voltage.

Conclusion

9. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

10. Any inquiry concerning this communication or earlier communications from

the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
June 20, 2005

MICHAEL T. TRAN
PRIMARY EXAMINER